

MOS FIELD EFFECT TRANSISTOR

2SK3482

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK3482 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

• Low On-State Resistance

 $R_{DS(on)1} = 29 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 10 \text{ V, ID} = 18 \text{ A)}$

RDS(on)2 = 34 m Ω MAX. (VGS = 4.5 V, ID = 18 A)

- Low Ciss : Ciss = 3600 pF TYP.
- Built-in Gate Protection Diode
- TO-251/TO-252 package

ORDERING INFORMATION

PART NUMBER	PACKAGE		
2SK3482	TO-251		
2SK3482-Z	TO-252		

(TO-251)

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage	Voss	100	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC)	ID(DC)	±36	Α
Drain Current (Pulse) Note1	D(pulse)	±144	Α
Total Power Dissipation (Tc = 25°C)	PT	50	W
Total Power Dissipation (T _A = 25°C)	PT	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	IAS	T.B.D. Note3	Α
Single Avalanche Energy Note2	Eas	T.B.D. Note3	mJ



(TO-252)



Notes 1. PW \leq 10 μ s, Duty cycle \leq 1 %

2. Starting Tch = 25°C, RG = 25 Ω , VGS = 20 V \rightarrow 0 V

3. T.B.D.: To be determined

THERMAL RESISTANCE

Channel to Case 2.5 °C/W Rth(ch-C) Channel to Ambient 125 °C/W Rth(ch-A)

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

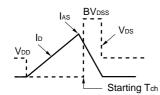


ELECTRICAL CHARACTERISTICS (TA = 25 °C)

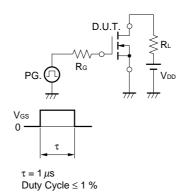
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, Ip = 18 A		23	29	mΩ
	RDS(on)2	V _G S = 4.5 V, I _D = 18 A		25	34	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 18 A	20	40		S
Drain Leakage Current	IDSS	V _{DS} = 100 V, V _{GS} = 0 V			10	μΑ
Gate to Source Leakage Current	lgss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Input Capacitance	Ciss	V _{DS} = 10 V		3600		pF
Output Capacitance	Coss	V _G s = 0 V		360		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		180		pF
Turn-on Delay Time	td(on)	ID = 18 A		20		ns
Rise Time	tr	V _{GS(on)} = 10 V		10		ns
Turn-off Delay Time	t d(off)	V _{DD} = 50 V		60		ns
Fall Time	t _f	$R_G = 1 \Omega$		10		ns
Total Gate Charge	Q _G	ID = 36 A		65		nC
Gate to Source Charge	Qgs	V _{DD} = 80 V		10		nC
Gate to Drain Charge	Q _{GD}	V _{GS(on)} = 10 V		18		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 36 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 36 A, VGS = 0 V		88		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		170		nC

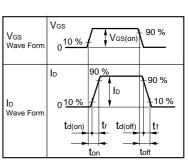
TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c} \text{D.U.T.} \\ \text{RG} = 25 \ \Omega \\ \text{PG.} \\ \text{V}_{\text{DD}} \\ \end{array}$



TEST CIRCUIT 2 SWITCHING TIME



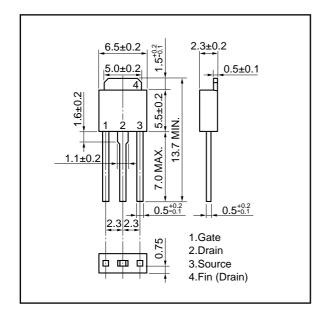


TEST CIRCUIT 3 GATE CHARGE

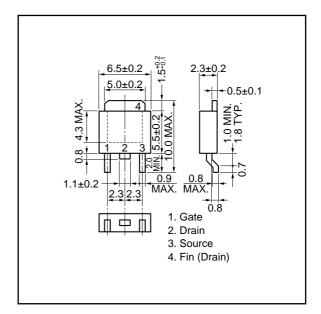


PACKAGE DRAWINGS (Unit: mm)

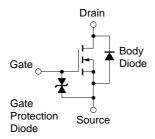
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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